**Lab 6 Report**

**Name: Aryan Agarwal**

**UT EID: aab5473**

**Section: MW 11 – 12:30**

A diagram of a software development

Description automatically generated

**Part 1**

**A diagram of a graph

Description automatically generated with medium confidence**

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**Part 2**

Verilog:

`timescale 1ns / 1ps

module Modes(

input clk,

input reset,

input ss,

input [1:0] modeSwitch,

input [3:0] A, B,

output wire [3:0] an,

output wire [0:0] dp,

output wire [6:0] sseg

);

reg [13:0] timeVal = 0;

reg [1:0] state = 0;

reg [1:0] next\_state = 0;

reg [1:0] modeState = 0;

wire [6:0] in0, in1, in2, in3;

hexto7segment c1 (.x(timeVal/1000 % 10), .r(in3));

hexto7segment c2 (.x(timeVal/100 % 10), .r(in2));

hexto7segment c3 (.x(timeVal/10 % 10), .r(in1));

hexto7segment c4 (.x(timeVal % 10), .r(in0));

wire slow\_clk1;

wire slow\_clk2;

reg [3:0] Aval = 0;

reg [3:0] Bval = 0;

clkdiv cl1(clk, reset, slow\_clk1);

clkdiv2 cl2(clk, reset, slow\_clk2);

time\_mux\_state\_machine c6(

.clk (slow\_clk1),

.reset (reset),

.in0 (in0),

.in1 (in1),

.in2 (in2),

.in3 (in3),

.an (an),

.sseg (sseg),

.dp(dp));

always @(posedge slow\_clk2 or posedge reset) begin

if (reset) begin

state <= 2'b00;

next\_state <= 2'b00;

if (modeSwitch == 2'b00)

timeVal <= 13'b0;

else if (modeSwitch == 2'b01 || modeSwitch == 2'b11) begin

if (8\*A[3] + 4\*A[2] + 2\*A[1] + A[0] <= 9)

Aval = 8\*A[3] + 4\*A[2] + 2\*A[1] + A[0];

if (8\*B[3] + 4\*B[2] + 2\*B[1] + B[0] <= 9)

Bval = 8\*B[3] + 4\*B[2] + 2\*B[1] + B[0];

timeVal <= 10\*(Aval) + Bval;

end

else if (modeSwitch == 2'b10)

timeVal <= 9999;

end

else begin

case (state)

2'b00 : begin

if (modeSwitch == 2'b00 || modeSwitch == 2'b01) begin

if (ss \* (timeVal < 9999))

next\_state = 2'b01;

else

next\_state = 2'b00;

end

else if (modeSwitch == 2'b10 || modeSwitch == 2'b11) begin

if (ss \* (timeVal > 0))

next\_state = 2'b01;

else

next\_state = 2'b00;

end

end

2'b01 : begin

if (modeSwitch == 2'b00 || modeSwitch == 2'b01) begin

timeVal = timeVal + 1;

if (!ss \* (timeVal < 9999))

next\_state = 2'b01;

else

next\_state = 2'b00;

end

else if (modeSwitch == 2'b10 || modeSwitch == 2'b11) begin

timeVal = timeVal - 1;

if (!ss \* (timeVal > 0))

next\_state = 2'b01;

else

next\_state = 2'b00;

end

end

default : begin

next\_state = 2'b00 ;

state = 2'b00;

end

endcase

state <= next\_state;

end

end

endmodule

Constraints:

set\_property PACKAGE\_PIN W5 [get\_ports clk]

set\_property IOSTANDARD LVCMOS33 [get\_ports clk]

create\_clock -add -name sys\_clk\_pin -period 10.00 -waveform {0 5} [get\_ports clk]

#7 segment display

set\_property PACKAGE\_PIN W7 [get\_ports {sseg[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[0]}]

set\_property PACKAGE\_PIN W6 [get\_ports {sseg[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[1]}]

set\_property PACKAGE\_PIN U8 [get\_ports {sseg[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[2]}]

set\_property PACKAGE\_PIN V8 [get\_ports {sseg[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[3]}]

set\_property PACKAGE\_PIN U5 [get\_ports {sseg[4]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[4]}]

set\_property PACKAGE\_PIN V5 [get\_ports {sseg[5]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[5]}]

set\_property PACKAGE\_PIN U7 [get\_ports {sseg[6]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {sseg[6]}]

set\_property PACKAGE\_PIN U2 [get\_ports {an[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[0]}]

set\_property PACKAGE\_PIN U4 [get\_ports {an[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[1]}]

set\_property PACKAGE\_PIN V4 [get\_ports {an[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[2]}]

set\_property PACKAGE\_PIN W4 [get\_ports {an[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {an[3]}]

set\_property PACKAGE\_PIN V7 [get\_ports dp]

set\_property IOSTANDARD LVCMOS33 [get\_ports dp]

#Buttons

set\_property PACKAGE\_PIN U18 [get\_ports reset]

set\_property IOSTANDARD LVCMOS33 [get\_ports reset]

set\_property PACKAGE\_PIN T18 [get\_ports ss]

set\_property IOSTANDARD LVCMOS33 [get\_ports ss]

#Mode

set\_property PACKAGE\_PIN R2 [get\_ports {modeSwitch[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {modeSwitch[1]}]

set\_property PACKAGE\_PIN T1 [get\_ports {modeSwitch[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {modeSwitch[0]}]

## Switches

## Connects pin V17 (SW0 on the board) to input a in our gate module

set\_property PACKAGE\_PIN V17 [get\_ports {B[0]}]

## Sets the switch to use 3.3V logic

set\_property IOSTANDARD LVCMOS33 [get\_ports {B[0]}]

## Connects pin V16 (SW1 on the board) to input b in our gate module

set\_property PACKAGE\_PIN V16 [get\_ports {B[1]}]

## Sets the switch to use 3.3V logic

set\_property IOSTANDARD LVCMOS33 [get\_ports {B[1]}]

set\_property PACKAGE\_PIN W16 [get\_ports {B[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {B[2]}]

set\_property PACKAGE\_PIN W17 [get\_ports {B[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {B[3]}]

set\_property PACKAGE\_PIN W15 [get\_ports {A[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {A[0]}]

set\_property PACKAGE\_PIN V15 [get\_ports {A[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {A[1]}]

set\_property PACKAGE\_PIN W14 [get\_ports {A[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {A[2]}]

set\_property PACKAGE\_PIN W13 [get\_ports {A[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {A[3]}]